PRACTICE PROBLEMS

PROBLEM 1

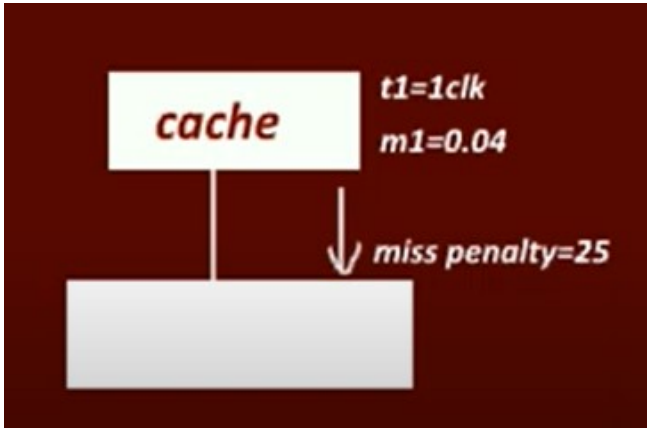
- Given the following, determine size of the sub-fields (in bits) in the address for direct mapping.
- We have 256 MB main memory and 1 MB cache memory
- The block size is 128 bytes

PROBLEM 2

A disk unit has 24 recording surfaces. It has a total of 14000 cylinders. There is an average of 400 sectors per track. Each sector contains 512 bytes of data. What is the data transfer rate at a rotational speed of 7200 r.p.m?

PBM 3

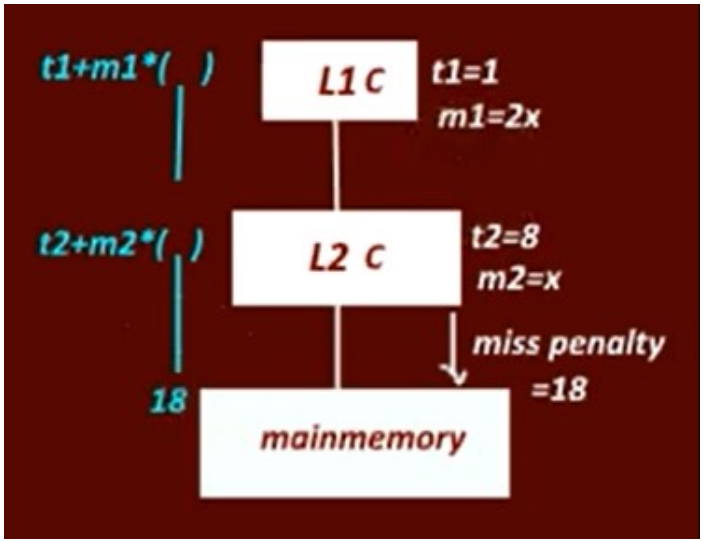
Find the average memory access time for a process with 2ns clock cycle time,a miss rate 0f 0.04 misses per instruction, a miss penalty of 25 clock cycles and a cache access time of 1 clock cycle.



AMAT=hit time+miss rate*miss penalty

Pbm 4

- In a two-level cache system, the access times of L1 and L2 1 and 8 clock cycles, respectively. The miss penalty from the L2 cache to main memory is 18 clock cycles. The miss rate of L1 cache is twice that of L2. The average memory access time(AMAT) of this cache system is 2 cycles. The miss rates of L1 and L2 respectively are:



AMAT = Access time of L1 + (MissRate L1 * miss penalty $L_{1)}$ **where miss penalty L1 = Access time of L2 + (MissRate L2 * miss penalty L2)**